Survey on the Usage and Assurance of Programmable Logic at NASA Centers

Note: Please return completed questionnaires directly to the contact person listed at the end of this survey. Partial submissions will be gladly accepted.

Purpose

Programmable Logic devices are becoming common within NASA projects and facilities. Programmable Logic Controllers often replace older control systems. Programmable Logic chips, such as FPGAs, are used to create custom capabilities within instrumentation. While essentially "hardware" devices, they are programmed like software. This hybrid aspect of Programmable Logic may not be fully addressed when the devices are assured.

This questionnaire will provide a broad picture of where Programmable Logic devices are used throughout NASA and how these various devices are assured for functionality, reliability, and safety. A cross-section of all Centers, programs, and facilities is required to provide accurate NASA-wide information.

The results of this questionnaire will be used as guidance for the creation of an Assurance Guidebook for Programmable Logic devices. Summaries of the information may be presented at technical conferences or within technical papers.

This questionnaire is part of an ongoing research project funded by the NASA IV&V Center through a Center Initiative. The Principal Investigator (PI) has produced this survey to obtain information on Programmable Logic usage throughout NASA and the processes used to assure those devices.

Background

Until recently, there was a reasonably clear distinction between hardware and software. Hardware was the pieces-parts: transistors, resistors, integrated circuits, etc. Software ran on the hardware (operating systems, applications programs) or resided *inside* the hardware (firmware).

Programmable logic blurs the lines between hardware and software. While the result is "hardware", they use a programming language to express the hardware relationships (like "software"). Two distinct categories of devices are included within the broad category of Programmable Logic: Programmable Logic Controllers (PLCs) and Programmable Logic Devices (PLDs).

A PLC is a special purpose computer having a central processing unit (CPU), power supply, a programming panel and/or interface to a programming system, inputs, and outputs. A PLC should also provide the capability to support remote I/O, special purpose I/O, I/O housings, connection, cables, additional power supplies, communication boards etc. A PLC is sometimes called a "programmable controller".

PLCs are used to control other equipment, such as production-line instrumentation or wind tunnels. They are programmed to perform their control function, usually in a ladder diagramming language. Conventional programming languages, such as BASIC, and other textual or graphical languages are becoming more commonly used in PLC programming.

PLDs are defined as devices with configurable logic gates and flip-flops, linked together with programmable interconnects. Memory cells control and define the function that the logic performs and how the logic gates are interconnected. Circuitry is developed in a programming language (such as VHDL [Very High Speed Integrated Circuit (VHSIC) Hardware Description Language] or Verilog), run on a simulator, compiled, and downloaded to the programmable device (PLDs). Simple PLDs have fewer than 500 logic gates while complex PLDs, such as CPLDs and FPGAs, can have 500 to more than 100,000 logic gates. While the resulting device is "hardware", the process of programming or designing it is "software". Some versions of programmable devices can even be changed "on the fly", such as CPLDs or FPGAs, though others, such as application specific integrate circuit (ASIC) devices, can only be programmed externally.

The variety of PLDs include:

- Field Programmable Gate Array (FPGA)
- Complex Programmable Logic Device (CPLD)
- PAL (Programmable Array Logic)
- GAL (Generic Array Logic)
- PLA (Programmable Logic Array)
- EPLD (Erasable Programmable Logic Device)
- EEPLD (Electrically-Erasable Programmable Logic Device)
- MAX (Multiple Array matrix)

Assurance is defined as "those activities that demonstrate the conformance of a product or process to a specified criteria (such as a functional requirement or a standard)." [from NASA Software Assurance Standard, NASA-STD-2201-93] Specific assurance activities vary with the discipline performing the assurance function. Activities usually include testing, documentation review (e.g. plans, requirements, schematics, software design diagrams), and process audits.

Confidentiality

Any personal information gathered as a direct or indirect result of this questionnaire will remain confidential. Summary information from the survey will not identify any individual, project, program, or facility, unless permission to do so is granted. Providing personal information is not necessary to complete the questionnaire.

Contact information is requested from those who are willing to be interviewed regarding their usage or assurance of Programmable Logic devices.

Instructions

Please complete this questionnaire if your project, program, or facility is using, or is planning to use, Programmable Logic, as defined in the ***Background*** section above. Examples of Programmable Logic include: FPGAs, Programmable Logic Controllers (PLCs), PLAs, and EPLDs.

Please feel free to add to, change, or otherwise alter the survey format to convey the information you wish to express. Complete as much of the questionnaire as is appropriate for your level of involvement with Programmable Logic. Feel free to add comments or additional information.

You may reply in any format by contacting Kalynnda Berens via email at **Kalynnda.Berens@grc.nasa.gov**. Further contact information can be found on the last page of this questionnaire.

Questions

1. General Information

NASA Center _____

Organization Code _____

Contractor? __ No __ Yes Company: _____

Position Description (e.g. engineer, project manager) _____

2. Name of Project, Program or Facility (hereafter referred to as *location*)

_____

3. Is Programmable Logic (as defined in the **Background** section) currently used at your location?

__ Yes __ No

Is Programmable Logic being considered for use in the future? __ Yes __ No

If you answered No to both questions above, you do not need to return this survey, though you may do so if you wish. Thank you for your time.

4. What types of Programmable Logic are used (or are being considered for use) at your location? Please check all that apply.

__ Programmable Logic Controller (PLC)

__ Field Programmable Gate Array (FPGA)

__ Programmable Array Logic (PAL)

__ Generic Array Logic (GAL)

__ Programmable Logic Array (PLA)

__ Erasable Programmable Logic Device (EPLD)

__ Multiple Array Matrix (MAX)

__ Electrically-Erasable Programmable Logic Device (EEPLD)

__ Complex Programmable Logic Device (CPLD)

__ System-on-a-chip (SoC)

__ Application Specific Integrated Circuit (ASIC)

__ Other _____

5. What is the Programmable Logic used for (or will be used for)? Examples are: control of facility, part of flight instrument, test equipment, etc.

_____

_____

_____

6. Do you personally work with the Programmable Logic (PL)? __ Yes __ No

If yes, do you (or will you):

__ Use the PL device

__ Program the PL device

__ Assure the PL device. This includes testing, process audits, and other assurance activities.

__ Other _____

7. At your location, who writes the Programmable Logic code?

__ Hardware Engineer

__ Software Engineer

__ Specialist in Programmable Logic devices.

__ Local Computer Science (on-center) organization

__ Outside source (off-center): _____

__ Other _____

8. What programming languages or design environments are used with the Programmable Logic? Examples include: VHDL, Verilog, LadderLogic, Basic, schematic design, etc.

_____

_____

_____

Assurance

9. Are any formal standards followed in the design or programming of the Programmable Logic? Standards may be military, safety-related (e.g. IEC 1131-3), or from other sources. __ Yes __ No

If yes, please list the standard(s): _____

10. Are there defined procedures or process for Programmable Logic software development or chip design?

__ Yes __ No

If yes, please briefly describe them:

_____

_____

11. Are project-developed standards or guidelines for design or coding used for Programmable Logic development? __ Yes __ No

12. Is the source code, logic diagram, schematic, or other programming information kept within a configuration management system? __ Yes __ No

13. How is the Programmable Logic tested?

Who performs the testing?

14. Does your Center Software Assurance group, or other Assurance organization, perform any of the following activities for Programmable Logic devices? Please check all that apply.

__ Review the source code (or visual diagram) __ Audit development process

__ Witness PLC physical programming __ Witness PL testing

__ Verify version information __ Audit configuration management

__ Other activities:

Name of Assurance organization:

Safety

15. At your location, what would be the consequences if the Programmable Logic device fails, assuming no backup devices or human intervention? Consequences could be death or injury, damage to facility, destruction of equipment, failed experiment, minor inconvenience, etc.

If the Programmable Logic device cannot lead to a hazard or safety-related situation, skip questions 16 and 17.

16. If the Programmable Logic device fails, how are "bad consequences" prevented? Examples are: hardware to prevent hazard, operator override, software monitoring and override, etc.

17. What safety approval process is used for the project, program, or facility that the Programmable Logic device is part of?

Please add any additional comments or information on the use or assurance of Programmable Logic devices at your location.

Personal Information

If you are willing to be contacted for follow-up questions, please provide contact information below:

Your Name: _____

Email: _____

Phone: _____ (optional)

Preferred contact method: __ Email __ Phone __ Other: _____

If you know someone who has knowledge of how Programmable Logic is used or assured within NASA, please send them a copy of this questionnaire, or provide contact information:

Name of Contact: _____

Organization: _____

Email: _____

Phone: _____ (optional)

Survey Questionnaire Return Information

Surveys can be returned via email to **Kalynnda.Berens@grc.nasa.gov**.

Due to NASA security regulations, an address for mailing hardcopies cannot be provided in this form. Please contact the researcher via email or phone to obtain a mailing address.

For further information, to convey answers verbally, or to discuss any of the questions in more detail, please contact the researcher directly.

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